This listing of the claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

1. (Currently amended) A method of forming a microelectronic structure comprising:

providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal gate directly disposed on a high k gate dielectric layer, and wherein the metal gate comprises at least one of platinum, ruthenium, palladium, and wherein a spacer is in direct contact with the metal gate, and

laser annealing the substrate.

2. (Previously presented) The method of claim 1 further comprising wherein the metal gate comprises a work function from about 3.9 electron volts to about 5.2 electron volts that is disposed on the gate dielectric layer.

3. (Canceled)

4. (Previously presented) The method of claim 1 further comprising wherein the metal gate does not substantially diffuse into a polysilicon layer disposed on the metal gate.

5. (Previously presented) The method of claim 1 wherein laser annealing the substrate comprises exposing the substrate to a laser beam for a time sufficient to activate an

implanted species.

6. (Original) The method of claim 1 wherein laser annealing the substrate comprises exposing the substrate to a laser beam pulsed at about 20 nanosecond intervals or less.

7. (Original) The method of claim 1 wherein laser annealing the substrate comprises activating an implanted species in the source/drain regions by laser annealing.

8. (Previously presented) The method of claim 7 further comprising wherein the ratio of the depth of the source/drain regions to the length of the source/drain regions is less than about 1:2.

9. (Canceled)

10. (Canceled)

11. (Currently amended) A method of forming a microelectronic structure comprising;

providing a substrate comprising doped source/drain and gate regions, wherein the gate region comprises a metal gate directly disposed on a high k dielectric layer, and wherein the metal gate comprises a work function approximately equal to a work function of one of an NMOS gate electrode ~~n doped polysilicon~~ and a PMOS gate electrode ~~p doped polysilicon~~, and

wherein the metal gate comprises at least one of platinum, ruthenium, palladium, and wherein a spacer is in direct contact with the metal gate; and

forming shallow source/drain regions by laser annealing the substrate.

12. (Original) The method of claim 11 wherein forming shallow source/drain regions comprises forming source/drain regions wherein the ratio of the depth of the source/drain regions to the length of the source/drain regions is less than about 1:2.

13. (Previously presented) The method of claim 11 further comprising wherein the metal gate comprises a work function from about 3.9 to about 4.2 electron volts.

14. (Canceled)

15. (Previously presented) The method of claim 11 further comprising wherein the metal gate comprises a work function from about 4.8 to about 5.1 electron volts.

16. (Previously presented) The method of claim 11 further comprising wherein the high k dielectric layer selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide and /or combinations thereof.

25. (Previously presented) The method of claim 1 wherein the metal gate does not substantially diffuse into the high k gate dielectric layer

Claims 17-24 (Canceled).